What Is Claimed Is:

1. A low-voltage-triggered electrostatic discharge (LVTESD) protection circuit, coupled to a pad of an integrated circuit (IC) to protect core circuits of the IC from ESD event, the ESD protection circuit comprising:

a semiconductor substrate having the first conductivity type;

an well region having the second conductivity type, formed in the semiconductor substrate;

an anode doped region having the first conductivity type, formed in the well region;

a gate structure, formed in the semiconductor substrate and outside the well region, the gate structure having a first side and a second side;

a first doped region having the second conductivity type, formed between the well region and the gate structure, immediately adjacent to the first side of the gate structure in the semiconductor substrate;

a second doped region having the second conductivity type, formed next to the second side of the gate structure in the semiconductor substrate; and

a plurality of isolated islands distributed in the first doped region so that the resistance of the first doped region is increased.

2. The ESD protection circuit in claim 1, wherein the ESD protection circuit further comprises:

a first contact region having the first conductivity type, formed in the semiconductor substrate; and

a second contact region having the second conductivity type, formed in the well region;

wherein the first contact region is coupled to the second doped region and a power pad of the IC, and the anode doped region is coupled to the pad.

3. The ESD protection circuit in claim 1, wherein the second contact region is coupled to the anode doped region.

4. The ESD protection circuit in claim 1, wherein the gate structure has an oxide layer formed on the semiconductor substrate, and a polysilicon layer formed on the oxide layer.

5. The ESD protection circuit in claim 4, wherein the polysilicon layer is coupled to the second doped region.

6. The ESD protection circuit in claim 1, wherein each of the isolated islands comprises an oxide layer formed on the semiconductor substrate, and a polysioicon layer formed on the oxide layer.

7. The ESD protection circuit in claim 1, wherein the isolated islands are field oxide.

8. The ESD protection circuit in claim 1, wherein each of the isolated islands has approximately the same width.

9. The ESD protection circuit of claim 1, wherein each of the isolated islands is elongated and approximately parallel to the first side of the gate structure.

10. The ESD protection circuit of claim 1, wherein each of the isolated islands is elongated and approximately perpendicular to the first side of the gate structure.

11. THE ESD protection circuit in claim 1, wherein the first type is a P-type, and the second conductivity type is an n-type.

12. A low-voltage-triggered electrostatic discharge (LVTESD) protection circuit, coupled to a pad of an integrated circuit (IC) to protect the core circuit of the IC from ESD stress, the LVTESD protection circuit comprising:

a semiconductor control rectifier, comprising an anode, a anode gate, a cathode and a cathode gate, the anode is coupled to the pad; and

a metal-oxide-semiconductor (MOS) having a second conductivity type, formed on a semiconductor substrate having a first conductivity type comprising a well having the second conductivity type, the MOS comprising:

a gate structure, formed on the semiconductor substrate, having a first side and a second side;

a first doped region, formed in the semiconductor substrate between the well and the gate structure and immediately adjacent to the first side of the gate structure, comprising at least one contact region coupled to the anode gate;

a second doped region, formed in the semiconductor substrate adjacent to the second side of the gate structure, and coupled to the cathode; and

a plurality of isolated islands, formed between the contact region and the first side of the gate structure in the first doped region, resulting in increased resistance of the first doped region.

13. The ESD protection circuit in claim 12, wherein each of the isolated islands comprises an oxide layer on the

semiconductor substrate, and a polysilicon layer on the oxide layer.

14. The ESD protection circuit in claim 12, wherein the IC further comprises a plurality of oxide layers, and each of the isolated islands is formed by one of the oxide layers.

15. The ESD protection circuit in claim 12, wherein each of the isolated islands has approximately the same length.

16. The ESD protection circuit in claim 12, wherein each of the isolated islands has an elongated profile and is approximately parallel to the first side of the gate structure.

17. The ESD protection circuit in claim 12, wherein each of the isolated islands has an elongated profile and is approximately perpendicular to the first side of the gate structure.

18. The ESD protection circuit in claim 12, wherein the first conductivity type is a p type, and the second conductivity type is an n type.